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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.
09/308,478	05/17/99	WEVER	U P99.0886

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EXAMINER	
SERGENT, D	
ART UNIT	PAPER NUMBER
2123	5

DATE MAILED: 05/24/01

Please find below and/or attached an Office communication concerning this application or proceeding.

Commissioner of Patents and Trademarks

Office Action Summary	Application No. 09/308,478	Applicant(s) WEVER ET AL.	
	Examiner Douglas W. Sergent	Art Unit 2123	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136 (a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____ .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-10* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-10* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claims _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are objected to by the Examiner.

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. § 119

13)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☒ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgement is made of a claim for domestic priority under 35 U.S.C. § 119(e).

Attachment(s)

15) ☒ Notice of References Cited (PTO-892)
16) ☒ Notice of Draftsperson's Patent Drawing Review (PTO-948)
17) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) *3* .
18) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
19) ☐ Notice of Informal Patent Application (PTO-152)
20) ☐ Other: .

DETAILED ACTION

1. Claims 1-10 have been examined in this application.

Specification

2. The disclosure is objected to because of the following informalities:

- The specification is not divided into standard sections as per U.S. Patent convention including: Background of the Invention, Summary of the Invention, Brief Description of the Drawings, Description of the Preferred Embodiment.
- The specification includes citation of references that is not in conformance with standard U.S. Patent format. References are cited (for example pg. 2, lines 4, 8, 21, 23 etc.) which are listed on pg. 11 of the specification. None of these references show subject matter which is required to understand the invention and therefore are not required to be incorporated by reference. However, incorporation of the references as is does not conform to U.S. Patent practice. Appropriate correction is required.

3. The title of the invention is not descriptive. A new title is required that is clearly indicative of the invention to which the claims are directed.

The following title is suggested: COMPUTER IMPLEMENTED METHOD FOR PARTITIONING AN ELECTRICAL CIRCUIT DESICRIPTION FOR EFFICIENT SIMULATION ON PARALLEL COMPUTERS.

Claim Objections

4. Claim 1 is objected to because of the following informalities:

– The claim includes typographic mistakes. The claim recites "imaging the electrical circuit is imaged". The examiner has interpreted the claim to mean "the electrical circuit is imaged". Appropriate correction is required.

Claim Rejections - 35 USC § 112

5. The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

6. Claims 1, 3, 9 and 10 are rejected under 35 U.S.C. 112, first paragraph, as containing subject matter which was not described in the specification in such a way as to enable one skilled in the art to which it pertains, or with which it is most nearly connected, to make and/or use the invention.

The first claim describes imaging the electrical circuit onto a graph that exhibits the same topology. This step is described in the specification on pg. 5, beginning at line 14. The specification does not describe in sufficient detail how this imaging takes place. In particular, typically when an electrical circuit is mapped (imaged) onto a graph, the nodes of the graph represent the circuit element and the edges represent connections between the circuit elements. The current specification describes a process that treats the circuit elements as the graph edges, however this is not sufficiently described in a manner that would allow one skilled in the art to replicate the invention.

Claim number 3 recites grouping of elements according or a controlled source, connecting loops with a common voltage source, and assuring so short circuits arise. These elements are not taught in the specification.

Claims 9 and 10 recite a voltage source and resistor that are allocated to partitions. These steps are not sufficiently described in the specification.

7. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

8. Claim 1 is rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

- The claim recites "imaging the electrical circuit". This seems to correspond to "mapping the electrical circuit" whereby circuit elements are associated with particular elements in a graph representation. Use of the term "imaging" is not Standard English in this context. The examiner has interpreted "imaging" to mean "mapping".
- The claim recites a "calculation outlay" which is not a standard term in the art. The term is referring to computational requirement or CPU requirement. The term is meant to describe the prediction of how much computation effort will be required to perform a function, and has been interpreted as such. However, the term "calculation outlay" is not standard in the art and should be changed.

Claim Rejections - 35 USC § 101

9. 35 U.S.C. 101 reads as follows:

> Whoever invents or discovers any new and useful process, machine, manufacture, or composition of matter, or any new and useful improvement thereof, may obtain a patent therefor, subject to the conditions and requirements of this title.

10. Claims 1-10 are rejected under 35 U.S.C. 101, as failing to meet one or more guidelines enumerated in "Examination Guidelines for Computer-Related Inventions" (the "Guidelines"), published in the Federal Register and available on the World Wide Web at: http://www.uspto.gov/web/offices/com/hearings/software/analysis/computer.html

The proposed invention as disclosed in the specification:

- Does have a practical application
- Does disclose a practical application in the technological arts.

As per 35 USC 101 analysis guidelines, claims 1-10:

- Do not constitute a computer program per se, a data structure per se, non-functional descriptive material or a natural phenomenon.
- Do not constitute a series of steps to be performed on a computer.
- Do not present post-computer process activity.
- Do not present pre-computer process activity.
- **Do manipulate abstract idea without limitation to a practical application.**
- Do not claim a mathematical process.

The fact that the claimed invention does not demonstrate post-computer or pre-computer process activity and merely manipulates data without demonstration of practical applicability makes the invention non-statutory. The invention is directed to a method of partitioning a circuit description to allow for parallel simulation. However, the claims do not demonstrate this functionality and simply claim the partitioning of the circuit description without indicating any practicality for doing so. Therefore the results produced cannot be seen as useful or tangible.

Claim Rejections - 35 USC § 102

11. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in a patent granted on an application for patent by another filed in the United States before the invention thereof by the applicant for patent, or on an international application by another who has fulfilled the requirements of paragraphs (1), (2), and (4) of section 371(c) of this title before the invention thereof by the applicant for patent.

12. Claims 1-10 are rejected under 35 U.S.C. 102(e) as being anticipated by Hachiya (U.S. Patent 6,031,979).

Hachiya teaches a method for partitioning a circuit model to allow for simulation on parallel computers. Hachiya seeks to partition the circuit such that the connection between the sections is minimized and the size of each partition is such that each requires similar computation times (col. 3, lines 30-67). Specifically, Hachiya teaches mapping the circuit description to a directed graph (col. 4, line 14, and figures 4A and 4B). Hachiya uses a weighted value to determine computational load and uses the sum as a measure for partitioning the circuit (col. 7, weight is K_t; col. 10, line 10 describes summation). The method then couples remaining edges in the min-cut section (col. 7, line 34). Hachiya does not explicitly describe comparing the sum to a prescribed threshold, however, Hachiya does teach determining if the sub-circuit computation times are well balanced (col. 9, line 21) which demonstrated comparing the values either with each other or with come predetermined value, therefore the threshold is deemed to be inherent in Hachiya.

Conclusion

13. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

- Tse et al teaches a gain matrix for use in circuit partitioning.
- Kapoor teaches circuit partitioning for running on multiple FPGAs.
- Shakleford teahces general graph partitioning.
- Marks teaches graph partitioning.
- Hendrickson et al teaches partitioning using spectral load balancing.
- Kapp et al teaches cost function analysis for determining partition sizes.
- Peidnado et al teaches algorithm for analyzing parallel load imbalances.
- Buch et al teaches where partitioning takes place on parallel processors.

14. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Douglas W. Sergent whose telephone number is (703)306-5448. The examiner can normally be reached on M-F (6:30 - 4:00) First Friday Off.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Kevin Teska can be reached on (703)305-9704. The fax phone numbers for the organization where this application or proceeding is assigned are (703)308-1396 for regular communications and (703)308-1396 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703)305-5140.

Doug Sergent/DS
May 2, 2001

KEVIN J. TESKA
SUPERVISORY
PATENT EXAMINER